IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-30. (Canceled)

31. (Currently Amended) A method of manufacturing a semiconductor memory device, comprising:

forming first wiring above a semiconductor substrate;

forming a first insulating film on the first wiring;

forming second and fourth wiring on the first insulating ~~insulting~~ film, the fourth wiring being formed away from the second wiring with a first space therebetween;

partially forming a second insulating film on the first insulating film and on the second and fourth wiring to form a first trench in the first space;

forming first and second magneto resistive elements on two side surfaces of the first trench, the first magneto resistive element comprising a first magnetic layer and a first nonmagnetic layer, the first magnetic layer and the first nonmagnetic layer being formed in a direction perpendicular to the semiconductor substrate, the second magneto resistive element comprising a second magnetic layer and a second nonmagnetic layer, and the second magnetic layer and the second nonmagnetic layer being formed in the direction perpendicular to the semiconductor substrate;

removing the first insulating film from a bottom surface of the first trench between the first and second magneto resistive elements to form a contact hole which exposes a portion of the first wiring, and removing a portion of the second insulating film which is ~~are~~ positioned above the second and fourth wiring to form second and third trenches;

forming a contact in the contact hole, the contact being connected to the first wiring and to the first and second magneto resistive elements; and

forming third and sixth wiring in the second and third trenches, respectively, the third wiring being connected to the first magneto resistive element, and the sixth wiring being connected to the second magneto resistive element.

32. (Currently Amended) A method according to claim 31, wherein the formation of the first and second magneto resistive elements comprises:

forming a magnetic layer material on the bottom surface and two side surfaces of the first trench and on the second insulating film;

removing the magnetic layer material on the bottom surface of the first trench and on the second insulating film to form the first and second magnetic layers on the two side surfaces of the first trench;

forming a nonmagnetic layer material on the bottom surface of the first trench, on the side surfaces of the first and second magnetic layers, and on the second insulating film; and

removing the nonmagnetic layer material on the bottom surface of the first trench and on the second insulating film to ~~from~~ form the first and second nonmagnetic layers on the side surfaces of the first and second magnetic layers.

33. (Currently Amended) A method of manufacturing a semiconductor memory device according to claim 31, wherein at least the first and second magneto ~~magnetic~~ resistive elements or the contact is divided in units of cells.

34. (Original) A method of manufacturing a semiconductor memory device according to claim 31, further comprising forming the third and sixth wiring into predetermined shapes, and at the same time dividing at least the first and second magneto resistive elements or the contact in units of cells.

35. (Original) A method of manufacturing a semiconductor memory device according to claim 31, further comprising forming a fifth wiring away from the second or fourth wiring with a second space narrower than the first space therebetween, simultaneously with the formation of the second and fourth wiring.

36. (Original) A method of manufacturing a semiconductor memory device according to claim 35, further comprising forming seventh and eighth wiring simultaneously with the formation of the second, fourth, and fifth wiring, the seventh wiring being formed away from the fifth wiring with the first space therebetween, and the eighth wiring being formed away from the seventh wiring with the second space therebetween.

37. (Original) A method of manufacturing a semiconductor memory device according to claim 35, wherein the first and second magneto resistive elements are TMR elements in which the first and second nonmagnetic layers are tunnel junction layers.